IN THE CLAIMS

We claim:

1. A semiconductor device comprising:

a semiconductor body on a semiconductor substrate, said semiconductor body having a top surface and laterally opposite sidewalls;

a semiconductor capping layer formed on the top surface and on the sidewalls of said semiconductor body;

a gate dielectric layer formed on said semiconductor capping layer on said top surface and on said sidewalls of said semiconductor body;

a gate electrode having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and

a pair of source/drain regions formed in said semiconductor body on opposite sides of said gate electrode.

2. The semiconductor device of claim 1 wherein said semiconductor capping layer have a tensile stress.

3. The semiconductor device of claim 2 wherein said semiconductor capping layer has greater tensile stress on the sidewalls of said semiconductor body and then on the top surface of said semiconductor body.

4. The semiconductor device of claim 2 wherein said source/drain regions are n type conductivity.

5. The semiconductor device of claim 1 wherein said semiconductor substrate is a silicon substrate, wherein said semiconductor body is a silicon germanium alloy and wherein said semiconductor capping layer is a silicon film.

6. The semiconductor device of claim 1 wherein said semiconductor capping layer has a compressive stress.

7. The semiconductor device of claim 6 wherein said semiconductor capping layer has a greater compressive stress on the sidewalls than on the top surface of said semiconductor body.

8. The semiconductor device of claim 6 wherein said semiconductor substrate is a monocrystalline silicon substrate, wherein said semiconductor body comprises a silicon-carbon alloy and wherein said semiconductor capping is a silicon film.

9. The semiconductor device of claim 1 wherein said semiconductor substrate is a silicon substrate, wherein said semiconductor body is a silicon body, and wherein said semiconductor capping layer is a silicon capping layer.

10. A semiconductor device comprising:

a silicon germanium body formed on a silicon monocrystalline substrate, said silicon germanium body having a top surface and a pair of laterally opposite sidewalls;

a silicon film formed on said top surface and on said sidewalls of said silicon germanium body;

a gate dielectric layer formed on said silicon film on said top surface of said semiconductor body and on said silicon film on said sidewalls of said semiconductor body;

a gate electrode having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and

a pair of source/drain regions formed in said semiconductor body on opposite sides of said gate electrode.

11. The semiconductor device of claim 10 wherein said silicon film is formed thicker on the top surface of said semiconductor body than on the sidewalls of said semiconductor body.

12. The semiconductor device of claim 10 wherein said silicon film has a thickness between 50-300Å.

13. The semiconductor device of claim 10 wherein said silicon germanium alloy comprises between 5-40% germanium.

14. The semiconductor device of claim 13 wherein said silicon germanium alloy comprises approximately 15-25% germanium.

15. The semiconductor device of claim 10 wherein said source/drain regions are n type conductivity.

16. A semiconductor device comprising:

a silicon-carbon alloy body formed on a silicon monocrystalline substrate, said silicon carbon alloy body having a top surface and a pair of laterally opposite sidewalls;

a silicon film formed on said top surface and on said sidewalls of said silicon carbon alloy body;

a gate dielectric layer formed on said silicon film on said top surface of said silicon-carbon body and on said silicon film on said sidewalls of said silicon-carbon alloy body;

a gate electrode having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and

a pair of source/drain regions formed in said semiconductor body on opposite sides of said gate electrode.

17. The semiconductor device of claim 16 wherein said silicon film is formed to a thickness between 50-300Å.

18. The semiconductor device of claim 17 wherein said silicon film has a thickness between 50-300Å.

19. The semiconductor device of claim 16 wherein said source/drain regions are p type conductivity.

20. A method of forming a semiconductor device comprising:

forming a pair of isolation regions in a semiconductor substrate, said pair of isolation regions defining an active substrate region in said semiconductor substrate therebetween, said isolation region extending above said substrate;

forming a semiconductor film on said active region of said semiconductor substrate between said pair of isolation regions;

etching back said isolation regions to form a semiconductor body from said semiconductor film wherein said semiconductor body has a top surface and a pair of laterally opposite sidewalls;

forming a semiconductor capping layer on said top surface and said sidewalls of said semiconductor body;

forming a gate dielectric layer over said capping layer formed on said sidewalls of said top surface of said semiconductor body;

forming a gate electrode having a pair of laterally opposite sidewalls on and around said gate dielectric layer; and

forming a pair of source/drain regions in said semiconductor body on opposite sides of said gate electrode.

21. The method of claim 20 wherein said semiconductor film is selectively grown from said active region of said semiconductor substrate.

22. The method of claim 20 wherein said capping layer is selectively grown from said semiconductor body.

23. The method of claim 20 wherein said isolation regions are etched back with a wet etchant.

24. The method of claim 20 wherein said semiconductor capping layer has a tensile stress.

25. The method of claim 24 wherein said semiconductor capping layer has a greater tensile stress on the sidewalls of said semiconductor body than on the top surface of said semiconductor body.

26. The method of claim 24 wherein said source/drain regions are n type conductivity.

27. The method of claim 20 wherein said semiconductor substrate is a silicon substrate and wherein said semiconductor body is a silicon germanium alloy and wherein said semiconductor capping layer is silicon.

28. The method of claim 20 wherein said semiconductor capping layer has a compressive stress.

29. The method of claim 28 wherein said semiconductor capping layer has a greater compressive stress on the sidewalls than on the top surface of said semiconductor body.

30. The method of claim 28 wherein said semiconductor substrate is a monocrystalline silicon substrate, wherein said semiconductor body comprises a silicon-carbon alloy and wherein said semiconductor capping layer an expitaxial silicon.

31. The method of claim 28 wherein said source/drain regions are p type conductivity.

32. A method of forming a semiconductor device comprising:

forming a pair of spaced apart isolation regions in a semiconductor substrate, said spaced apart isolation regions defining an active substrate area in said substrate wherein said isolation regions extend above said active substrate area;

forming a semiconductor film on said active area of said substrate between said isolation regions;

forming a first capping layer on said top surface of said semiconductor film between said isolation regions;

etching back said isolation regions to form a semiconductor body having a top surface with said first capping layer and a pair of laterally opposite sidewalls;

forming a second capping layer on said first capping layer on the top surface of said semiconductor body and on said sidewalls of said semiconductor body;

forming a gate dielectric layer on said second capping layer on said first capping layer on said semiconductor body and on said second capping layer on said sidewalls of said semiconductor body;

forming a gate electrode having a pair of laterally opposite sidewalls on and around said gate dielectric layer; and

forming a pair of source/drain regions in said semiconductor body on opposite sides of said gate electrode.

33. The method of claim 32 wherein said first and second capping layer are epitaxial silicon and wherein said semiconductor body is a silicon germanium alloy and wherein said semiconductor substrate is a silicon monocrystalline substrate.

34. The method of claim 32 wherein said first and second capping layer are epitaxial silicon, wherein said semiconductor body is a silicon-carbon alloy and wherein said semiconductor substrate is a silicon monocrystalline substrate.

35. The method of claim 32 wherein said first and second semiconductor capping layers have a tensile stress.

36. The method of claim 32 wherein said first and second semiconductor capping layers have a compressive stress.

37. The method of claim 32 wherein said semiconductor film has a different lattice structure than said semiconductor substrate so that said semiconductor film has a stress formed therein.

38. A method of forming a semiconductor device comprising:

forming a first semiconductor body and a second semiconductor body on a substrate, said first and said second semiconductor bodies each having a top surface and a pair of laterally opposite sidewalls, said first semiconductor body and said second semiconductor body separated by a distance;

forming a semiconductor capping layer on said sidewalls and said top surface of said first and said second semiconductor bodies;

forming a gate dielectric layer on said top surface and said sidewalls of said first and said second semiconductor bodies; and

forming a gate electrode on said gate dielectric layer on said top surface of said first and second semiconductor bodies and adjacent to said gate dielectric layer on said sidewalls of said first and second semiconductor bodies.

39. The method of claim 38 wherein said semiconductor bodies are defined utilizing a photolithography process and wherein said distance separating said first and second bodies is the minimum dimension achievable by said photolithography process.

40. The method of claim 39 wherein said first and second semiconductor bodies having a width equal to the smallest dimension definable by said photolithography process.

41. The method of claim 38 wherein said semiconductor body is an epitaxial silicon film and wherein said semiconductor capping layer is an epitaxial silicon film.

42. The method of claim 38 wherein said semiconductor body is an epitaxial silicon germanium alloy film and wherein said semiconductor capping layer is an epitaxial silicon film.